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Xilinx DSP Targeted Design Platforms Deliver Performance, Price, Power, and Productivity

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Digital signal processing (DSP) design starts have surpassed every other segment of the processing arena. Consequently, the demand for differentiated value in every aspect of DSP design has never been higher, increasing pressure on the teams tasked to build winning designs in record time. Xilinx conceived the Targeted Design Platform to address this challenge—the necessity to do more with less, to remove risk wherever possible, and to differentiate in order to excel.

Introduction

Combining the inherent flexibility and performance of the FPGA with the increased productivity afforded by targeted platform-based design creates an optimal design scenario. For Xilinx DSP Targeted Design Platforms, this equates to the ability to optimize DSP processing and system performance, price/performance, and productivity for the broadest possible range of DSP designs and design team expertise.

Xilinx® FPGAs have already established a commanding role in a host of DSP-enabled applications where processing performance, I/O, and power requirements exceed the capabilities effectively delivered by discrete DSP devices. When price/performance represents a premium value for a DSP application, such as industrial or consumer video applications or automotive driver assist systems, Xilinx FPGAs have also demonstrated their viability versus discrete DSPs and ASSPs.

Xilinx continues to offer DSP design teams an unprecedented array of integrated platform elements that ensure optimal performance, price, and productivity with the introduction of three new DSP Targeted Design Platforms:

- A high-performance DSP platform based on the Virtex®-6 LX240T FPGA
- A cost-optimized DSP platform based on the Spartan®-6 LX150T FPGA
- A co-processing platform utilizing the Spartan-6 LX45T FPGA in conjunction with the Texas Instruments OMAP L-138 low-power applications processor

An overview of the methodology upon which each DSP Targeted Design Platform is built reveals its usability as a platform to accelerate the creation of successful DSP designs. Each DSP Targeted Design Platform kit contains:

- An FPGA suited to the class of design for which the kit was created
- A development board with industry-standard FPGA Mezzanine Card (FMC)⁽¹⁾ expansion slots for I/O mezzanine cards
- A full suite of design tools supporting the full range of engineering personas/preferences
- Intellectual Property (IP) blocks appropriate for the Targeted Design Platform
- A Targeted Reference Design suitable for the particular class of DSP design
- A demonstration program running on the Targeted Reference Design to accelerate development time
- Documentation and design files (Gerber files, schematics, user manual, etc.)

1. FMC - Developed by a consortium of companies ranging from FPGA vendors to end users, the FMC is an ANSI standard that provides a standard mezzanine card form factor, connectors, and modular interface to an FPGA located on a base board.

Avnet Virtex-6 FPGA DSP Kit with AD/DA

The new Virtex-6 FPGA DSP Development Kit (see [Figure 1](#)) targets applications that require high-end signal processing performance, such as:

- Aerospace and defense
- Medical technology
- High-performance computing
- Next-generation wireless communications

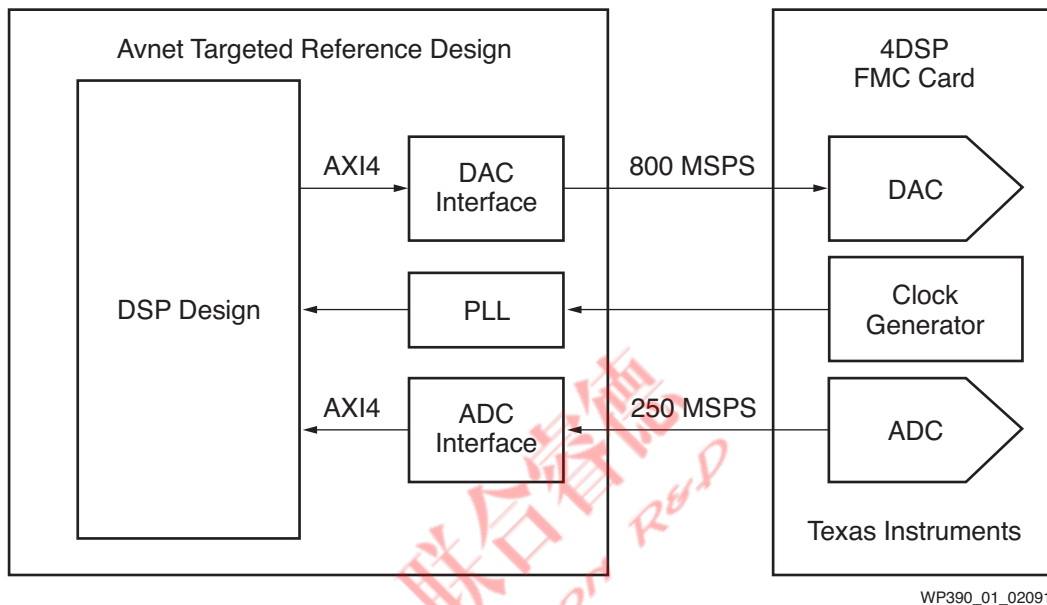


Figure 1: Virtex-6 FPGA DSP Kit Targeted Reference Design Block Diagram

The kit comes with an FMC designed by 4DSP (the FMC150 ADC/DAC mezzanine card) that integrates a Texas Instruments' dual-channel, 14-bit, 250 MSPS Analog-to-Digital Converter (ADC) and dual-channel, 16-bit, 800 MSPS Digital-to-Analog Converter (DAC) to enable customers to tune performance in both the analog and digital domains while saving weeks or months of development time.

The kit includes a DSP reference design that provides sample rate conversion to the high-speed data converters and allows for full configuration and control of the analog interface from the Virtex-6 FPGA (i.e., sampling frequency, analog input gain, offset correction, and clocking). This platform enables users to optimize both the hardware and software domains of their systems for the desired signal-to-noise ratio, quantization, analog filtering, and gain. The Targeted Reference Design also uses AXI4-Stream (an AMBA® specification), which is a high-performance, point-to-point interconnect used to reduce resource utilization without impacting performance. Through this interface, the kit also facilitates plug-and-play integration of AXI4-compliant third-party IP and high-level design flows.

The Virtex-6 FPGA DSP Development Kit supports design flows optimized for Register Transfer Language (RTL), System Generator for DSP⁽¹⁾, and C/C++. Users can easily modify the reference design to accommodate a different analog interface

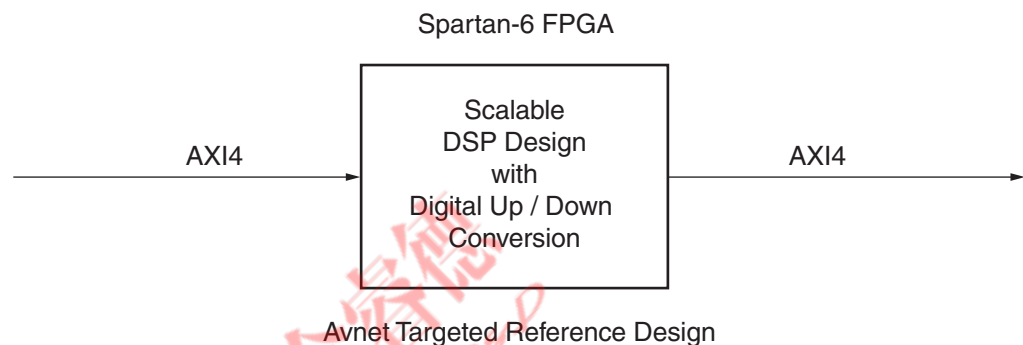
1. A Xilinx system-level modeling tool that provides automatically compiled high-level abstractions and access to underlying FPGA resources through low-level abstractions.

and then extend the design to implement a specific end-user application using their design flow of choice.

Avnet Spartan-6 FPGA DSP Kit

The new Spartan-6 FPGA DSP Development kit (see [Figure 2](#)) is an excellent entry-level platform for customers who want to add DSP to new or existing systems in the most cost and power-efficient manner possible. Markets for this kit include:

- Ultrasound equipment
- Consumer video devices
- Software defined radio
- Test and measurement



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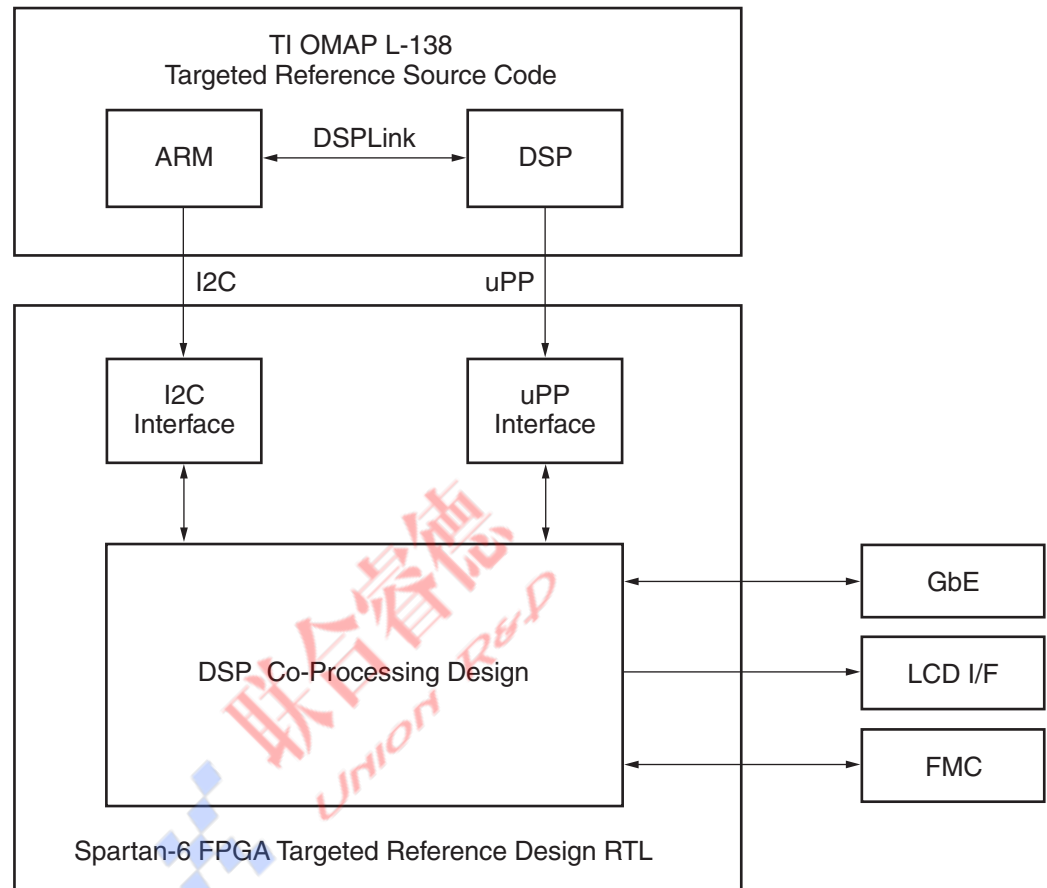
Figure 2: Spartan-6 FPGA DSP Kit Targeted Reference Design Block Diagram

The kit's development board features a Spartan-6 LX150T FPGA that delivers unmatched DSP performance per dollar. Offering over 40 times the processing performance and nearly seven times more performance/watt than discrete DSPs, the Spartan-6 LX150T FPGA also integrates serial transceivers for high-speed system connectivity.

In addition to a number of design tutorials, the kit includes the DSP Targeted Reference Design that is suitable for interfacing to high-speed analog and is easy to modify and extend within a preferred design environment, either RTL, Model-Based Design with System Generator for DSP, or untimed C/C++ synthesis. The latest version of the Xilinx ISE® Design Suite included in the kit supports the AXI4 stream interface that simplifies integration of DSP blocks with other system-level components.

Avnet TI OMAP/Spartan-6 FPGA Co-Processing Kit

Xilinx, Texas Instruments, and Avnet have collaborated to develop a co-processing platform that integrates the Texas Instruments OMAP L-138, dual-core applications processor with a Spartan-6 LX45T FPGA (see [Figure 3](#)).



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Figure 3: TI OMAP/Spartan-6 FPGA Co-Processing Kit Reference Design Block Diagram

The OMAP/Spartan-6 FPGA Co-Processing Kit provides the optimal balance of DSP, embedded ARM processing, and FPGA resources in a single integrated platform that enables OMAP developers to easily extend the capability of their systems using programmable logic.

The kit enables DSP software designers to boost performance by off-loading to the FPGA and accelerating high-performance DSP functions; the OMAP device can then perform system control and low-bandwidth processing functions more efficiently. The designer can easily explore and implement design partitioning trade-offs to achieve optimal system and DSP performance. All external I/O is routed through the FPGA, which helps users to leverage the flexibility of the Spartan-6 FPGA to expand the interface options of the OMAP device (e.g., interfaces for high-speed analog with parallel or serial interfaces, high-speed HD video, and output I/O for LCD monitors).

The kit includes a co-processing reference design to illustrate these performance boosting capabilities. Designers can get started quickly using familiar design environments.

The following traditional design flows are available for this platform:

- Texas Instruments Code Composer Studio for DSP software development
- RTL flow with reusable and extensible code
- RidgeRun SDK for embedded Linux development

The following high-level design flows are supported for this platform:

- MathWorks® Simulink® HDL Coder or System Generator for DSP: Model-based design for FPGA development
- MathWorks Real-Time Workshop: Model-based design for DSP software development
- AutoESL C/C++ to FPGA: Synthesis for FPGA Development

Tutorials

Xilinx offers a series of tutorials demonstrate essential DSP design techniques, including:

- Verifying DSP hardware against algorithmic system models
- Designing and programming filter coefficients
- Using FPGA parallelism for greater cost/performance
- Accelerating development using Xilinx DSP IP compilers
- Trading off fidelity vs. hardware efficiency
- Performing hardware accelerated co-simulation
- Incorporating C-Synthesis to FPGA design flow
- Interfacing to high-speed analog signals using DAC or ADC FMC connectors

The Ecosystem Steps Up

The two-fold scope of the DSP Targeted Design Platform vision is to deliver complete DSP platforms that efficiently cover the broadest possible DSP requirements and to offer design methodologies aligned to the way developers prefer to work. Xilinx has been able to achieve these goals with substantial contributions from an enthusiastic ecosystem that includes industry leaders like Texas Instruments, Avnet Electronics Marketing, MathWorks, and 4DSP.

Texas Instruments

Texas Instruments provides both the high-speed analog components and the OMAP applications processors included in the Xilinx DSP Platforms. The two companies have a long history of collaboration, and together with Avnet and MathWorks, have been instrumental in bringing easy-to-use DSP solutions to market.

Avnet Electronics Marketing

Avnet Electronics Marketing is a key ecosystem partner in the development of the Xilinx DSP Targeted Design Platform Kits, having designed boards and reference designs, ultimately bundling the Spartan-6 FPGA DSP Kit, the Virtex-6 FPGA DSP Kit with integrated ADC/DAC, and the Spartan-6 FPGA Co-Processing Development Kit. Avnet and Xilinx aligned their platform development strategies to maximize

application coverage and provide the most productive out-of-box experience available to DSP system designers.

MathWorks

MathWorks, a long-time industry collaborator with Xilinx, provides a model-based design environment that enables a variety of signal processing design personas to leverage the performance, cost, and power benefits of FPGAs in DSP systems. All Xilinx DSP development kits provide instructions for gaining access to MathWorks evaluation products.

4DSP

4DSP makes standardized FMC mezzanine cards that expand the capabilities of other base/carrier boards for key applications in specific markets. Working in collaboration with Texas Instruments and Xilinx, 4DSP has defined an interface that allows designers to control key settings on the data converter devices from within the FPGA. When combined with the ability to change digital filter characteristics within the FPGA, users can explore using both analog and digital optimizations simultaneously to achieve best results.

The FMC150 ADC/DAC mezzanine card is an integrated ADC/DAC card developed using this interface to compliment the high-performance Virtex-6 FPGA DSP Development Kit.

Summary

DSP has become an essential enabling technology for an extraordinarily large and expanding range of markets and applications. To accommodate such a varied market landscape with the right levels and combinations of performance, cost, power, and usability, Xilinx (in conjunction with its ecosystem partners) has created a portfolio of three DSP platform kits tailored to the requirements of three primary segments: high-performance, price/performance, and co-processing.

The Virtex-6 FPGA DSP Platform Kit addresses the need for very high DSP performance.

The Spartan-6 FPGA DSP Platform Kit is an excellent entry level platform that serves cost-optimized DSP applications in markets traditionally served by processors.

The TI OMAP/Spartan-6 FPGA Co-Processing Platform Kit enables developers to reduce or eliminate application bottlenecks using the Spartan-6 FPGA to achieve system accelerations, thereby boosting the performance or capabilities of their system processors without having to abandon their familiar development environments and legacy code.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
02/24/11	1.0	Initial Xilinx release.

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